**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claim 1 (currently amended): A digital signal delay device for converting a signal (IN) into a corresponding delayed signal (OUT), comprising a plurality of signal delay elements connected in series, wherein, as a function of the desired delay of the delayed signal (OUT), the respective output signal of a particular signal delay element is used for generating the delayed signal (OUT), wherein said signal delay elements each comprise one single inverter only,

wherein said signal delay elements are respectively connected with corresponding gates,

wherein as a function of the respectively desired delay, that gate is activated that is connected to the signal delay element whose output signal is to be used for generating the delayed signal (OUT),

wherein when the output signal of the particular signal delay element is inverted vis-à-vis the signal (IN), the gate connected with the particular signal delay element is designed such that the gate advances the output signal in an inverted manner and, when the output signal of the particular signal delay element is non-inverted vis-à-vis the signal (IN), the gate connected with the particular signal delay element is designed such that the gate advances the output signal in a non-inverted manner.

Claim 2 (currently amended): The digital signal delay device according to claim 1, wherein as a function of the respectively desired delay, the output signal of the ~~respective~~ particular signal delay element used for generating the delayed signal (OUT) is inverted or non-inverted vis-à-vis the signal (IN).

Claims 3-8 (canceled)

Claim 9 (currently amended): The digital signal delay device according to claim ~~8~~26, wherein the gates, depending on whether ~~they~~ the gates are connected with a signal delay element whose output signal is inverted or non-inverted vis-à-vis the signal (IN), [–]comprise an inverter circuit arrangement or a transfer gate circuit arrangement.

Claim 10 (currently amended): The digital signal delay device according to claim ~~8~~26, wherein the gates, depending on whether ~~they~~ the gates are connected with a signal delay element whose output signal is inverted or non-inverted vis-à-vis the signal (IN), [–]comprise two inverter circuit arrangements, or a transfer gate circuit arrangement and an inverter circuit arrangement.

Claim 11 (currently amended): The digital signal delay device according to claim ~~8~~26, wherein the gates, depending on whether ~~they~~ the gates are connected with a signal delay element whose output signal is inverted or non-inverted vis-à-vis the signal (IN), [–]comprise two inverter circuit arrangements and a transfer gate circuit arrangement, or three inverter circuit arrangements.

Claim 12 (original): The digital signal delay device according to claim 11, wherein at least one of the inverter circuit arrangements is a tristate inverter circuit arrangement.

Claims 13-20 (canceled)

Claim 21 (new): The digital signal delay device according to claim 1, wherein the gates, depending on whether the gates are connected with a signal delay element whose output signal is inverted or non-inverted vis-à-vis the signal (IN), comprise an inverter circuit arrangement or a transfer gate circuit arrangement.

Claim 22 (new): The digital signal delay device according to claim 1, wherein the gates, depending on whether the gates are connected with a signal delay element whose output signal is

inverted or non-inverted vis-à-vis the signal (IN), comprise two inverter circuit arrangements, or a transfer gate circuit arrangement and an inverter circuit arrangement.

Claim 23 (new): The digital signal delay device according to claim 1, wherein the gates, depending on whether the gates are connected with a signal delay element whose output signal is inverted or non-inverted vis-à-vis the signal (IN), comprise two inverter circuit arrangements and a transfer gate circuit arrangement, or three inverter circuit arrangements.

Claim 24 (new): The digital signal delay device according to claim 23, wherein at least one of the inverter circuit arrangements is a tristate inverter circuit arrangement.

Claim 25 (new): The digital signal delay device according to claim 1, wherein when the output signal of the particular signal delay element is inverted vis-à-vis the signal (IN), the gate connected with the particular signal delay element includes two n-channel field effect transistors and two p-channel field effect transistors, and when the output signal of the particular signal delay element is non-inverted vis-à-vis the signal (IN), the gate connected with the particular signal delay element includes one n-channel field effect transistor and one p-channel field effect transistor.

Claim 26 (new): A digital signal delay device for converting a signal (IN) into a corresponding delayed signal (OUT), comprising a plurality of signal delay elements connected in series, wherein, as a function of the desired delay of the delayed signal (OUT), the respective output signal of a particular signal delay element is used for generating the delayed signal (OUT), wherein said signal delay elements each comprise one single inverter only,

wherein said signal delay elements are respectively connected with corresponding gates,

wherein as a function of the respectively desired delay, that gate is activated that is connected to the signal delay element whose output signal is to be used for generating the delayed signal (OUT),

wherein when the output signal of the particular signal delay element is inverted vis-à-vis the signal (IN), the gate connected with the respective signal delay element is designed such that the gate advances the output signal in a non-inverted manner and, when the output signal of the particular signal delay element is non-inverted vis-à-vis the signal (IN), the gate connected with the respective signal delay element is designed such that the gate advances the output signal in an inverted manner.

Claim 27 (new): The digital signal delay device according to claim 26, wherein as a function of the respectively desired delay, the output signal of the particular signal delay element used for generating the delayed signal (OUT) is inverted or non-inverted vis-à-vis the signal (IN).

Claim 28 (new): The digital signal delay device according to claim 26, wherein when the output signal of the particular signal delay element is inverted vis-à-vis the signal (IN), the gate connected with the particular signal delay element includes one n-channel field effect transistor and one p-channel field effect transistor, and when the output signal of the particular signal delay element is non-inverted vis-à-vis the signal (IN), the gate connected with the particular signal delay element includes two n-channel field effect transistors and two p-channel field effect transistors.

Claim 29 (new): A digital signal delay device for converting an input signal into a corresponding delayed signal, the device comprising

a first signal delay element, including only one inverter, configured to receive the input signal;

a first gate, connected to the output of the first signal delay element, configured to output the delayed signal when the first gate is activated, the first gate including two p-channel field effect transistors and two n-channel field effect transistors, the gates of one of the two p-channel field effect transistors and one of the two n-channel field effect transistors connected with the other and with the input of the first gate, and the sources of the one of the two p-channel field

effect transistors and the one of the two n-channel field effect transistors connected with the other and with the output of the first gate;

a second delay element, connected in series with the first delay element, including only one inverter, configured to receive the output from the first signal delay element; and

a second gate, connected to the output of the second signal delay element, configured to output the delayed signal when the second gate is activated, the second gate including one p-channel field effect transistor and one n-channel field effect transistor, the drains of the one n-channel field effect transistor and the one p-channel field effect transistor connected with the other and with the output of the second gate, and the sources of the one n-channel field effect transistor and the one p-channel field effect transistor connected with the other and with the input of the second gate.